

## Education

### Carnegie Mellon University

Aug 2009 – Jul 2013,  
Jun 2015 – Feb 2019

Ph.D. Electrical & Computer Engineering

Thesis: *Finding and Exploiting Parallelism with Data-Structure-Aware Static and Dynamic Analysis*

Advisors: Profs. Todd C. Mowry and Phillip B. Gibbons

### Carnegie Mellon University

Aug 2009 – Dec 2011

M.S. Electrical & Computer Engineering

GPA: 4.000

### University of Notre Dame

Aug 2006 – May 2009

B.S. Computer Engineering, *summa cum laude*

GPA: 3.924

## Full-Time Work Experience

**F5** (San Jose, CA)

Senior Architect

Nov 2024 – present

- **WebAssembly and compilers expert** covering research and development in the Office of the CTO to evolve a standards-based, high-performance, secure WebAssembly platform and its associated compiler tooling.

**Fastly** (San Francisco, CA)

Principal Software Engineer

Apr 2022 – Nov 2024

Staff Software Engineer

Oct 2020 – Mar 2022

- **Tech lead for the Cranelift compiler** open-source project as part of the WebAssembly team for the Compute product, driving overall compiler quality. Rewrote compiler backend to improve compile-time and runtime performance significantly: built new register allocator, instruction selector DSL and metacompiler, and new mid-end optimization framework based on novel application of e-graphs. Mentored and onboarded contributors. Guided multi-organization collaborations and grew compiler to approximately 5 fulltime contributors, 4 supported ISAs, and comparable performance to peer JIT compilers (and average within 10% of LLVM with much faster compilation). Compiler ships in Wasmtime and also as an alternative backend for the Rust compiler.
- Developed **JS-to-Wasm ahead-of-time compiler** based on the SpiderMonkey JS engine. Began by porting SpiderMonkey to run inside a Wasm module. Added and upstreamed new interpreter tier (Portable Baseline) that supports inline-cache acceleration without requiring runtime code generation. Developed novel partial-evaluation compiler toolchain that combines interpreter with user code to produce compiled Wasm bytecode. Achieved 3-5x speedups with full compatibility. Gave several talks on novel approach with emphasis on correct-by-construction derivation.
- Contributed to **Wasmtime runtime**: used virtual-memory techniques and lazy initialization to achieve single-microsecond Wasm module instantiation times (400x improvement). Built lightweight compiler-based cooperative async scheduling.
- Focused on **correctness techniques**: proof-carrying code for sandboxing primitives, symbolic checker for register allocator, formal verification for compiler backend, rigorous fuzzing.
- Academic **research collaborations**: coauthored two ASPLOS papers ('23 and '24) on Wasm sandboxing and Cranelift formal verification. Gave invited keynote at EGRAPHS workshop on Cranelift's optimizer.

**Mozilla** (Mountain View, CA)

Senior Compiler Engineer

Aug 2019 – Oct 2020

- Advanced the **Cranelift JIT compiler** backend to provide production-grade WebAssembly support in **Firefox on aarch64 (ARM64)**, including developing a new aarch64 backend with a small team. Analyzed and carefully optimized to generate code that is competitive with other JITs.
- Worked on the **SpiderMonkey JavaScript JIT engine**.

**Google** (Mountain View, CA)

Software Engineer

Apr 2014 – May 2015

- Analyzed and enhanced performance of **Protocol Buffers**, a data serialization/marshalling framework used extensively in server-side infrastructure, by improving generated code and runtime library.

- Co-developed and led the release of **custom memory allocation (arena) support** for Protocol Buffers, saving significant CPU resources in production.
- Developed **Protocol Buffers bindings** as native-code plugins for Ruby and Node.js, and adapted a pure-JavaScript implementation for external release.

**Intel** (Hillsboro, OR)

Silicon Architecture Engineer

Aug 2013 – Apr 2014

- Worked on the core microarchitecture team for a **future-generation Atom core**.
- Defined **branch predictors** and related logic; worked with cycle-accurate simulator and estimated power and area.
- Worked with RTL engineers to specify implementation details and hand off documentation.

## Conference Publications

- [Chris Fallin](#), Maxwell Bernstein. “Partial Evaluation, Whole-Program Compilation.” In *PLDI 2025*, Seoul, South Korea, June 2025.
- Alexa VanHattum, Monica Pardeshi, [Chris Fallin](#), Adrian Sampson, Fraser Brown. “Lightweight, Modular Verification for WebAssembly-to-Native Instruction Selection.” In *ASPLOS 2024*, San Diego, CA, April 2024.
- Shravan Narayan, Tal Garfinkel, Mohammadkazem Taram, Joey Rudek, Daniel Moghimi, Evan Johnson, [Chris Fallin](#), Anjo Vahldiek-Oberwagner, Michael LeMay, Ravi Sahita, Dean Tullsen, Deian Stefan. “Going beyond the Limits of SFI: Flexible and Secure Hardware-Assisted In-Process Isolation with HFI.” In *ASPLOS 2023*, Vancouver, BC, Canada, March 2023.
- [Chris Fallin](#). “Safe, Flexible Aliasing with Deferred Borrows.” In *ECOOP 2020*, Virtual Conference, Nov 2020.
- [Chris Fallin](#), Chris Wilkerson, Onur Mutlu. “The Heterogeneous Block Architecture.” In *ICCD 2014*, Seoul, South Korea, Oct 2014.
- Rachata Ausavarungnirun, [Chris Fallin](#), Xiangyao Yu, Kevin Chang, Greg Nazario, Reetuparna Das, Gabriel Loh, Onur Mutlu. “Design and Evaluation of Hierarchical Rings with Deflection Routing.” In *SBAC-PAD 2014*, Paris, France, Oct 2014.
- Yoongu Kim, Ross Daly, Jeremie Kim, [Chris Fallin](#), Ji Hye Lee, Donghyuk Lee, Chris Wilkerson, Konrad Lai, Onur Mutlu. “Flipping Bits in Memory Without Accessing Them: An Experimental Study of DRAM Disturbance Errors.” In *ISCA-41*, Minneapolis, MN, Jun 2014.
- Vivek Seshadri, Yoongu Kim, [Chris Fallin](#), Donghyuk Lee, Rachata Ausavarungnirun, Gennady Pekhimenko, Yixin Luo, Onur Mutlu, Michael A. Kozuch, Phillip B. Gibbons, Todd C. Mowry. “RowClone: Fast and Energy-Efficient In-DRAM Bulk Data Copy and Initialization.” In *MICRO-46*, Davis, CA, Dec 2013.
- Kevin Chang, Rachata Ausavarungnirun, [Chris Fallin](#), Onur Mutlu. “HAT: Heterogeneous Adaptive Throttling for On-Chip Networks.” In *SBAC-PAD 2012*, New York, NY, Oct. 2012.
- George Nychis, [Chris Fallin](#), Thomas Moscibroda, Onur Mutlu, Srinivasan Seshan. “On-Chip Networks from a Networking Perspective: Congestion and Scalability in Many-core Interconnects.” In *ACM SIGCOMM 2012 (SIGCOMM)*, Helsinki, Finland, Aug. 2012.
- [Chris Fallin](#), Greg Nazario, Xiangyao Yu, Kevin Chang, Rachata Ausavarungnirun, Onur Mutlu. “MinBD: Minimally-Buffered Deflection Routing for Energy-Efficient Interconnect.” In *6th ACM/IEEE International Symposium on Networks-on-Chip (NOCS)*, Lyngby, Denmark, May 2012. *One of five papers nominated for Best Paper award.*
- Eiman Ebrahimi, Rustam Miftakhutdinov, [Chris Fallin](#), Chang Joo Lee, Onur Mutlu, Yale Patt. “Parallel Application Memory Scheduling.” In *44th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, Porto Alegre, Brazil, Dec. 2011.
- Howard David, [Chris Fallin](#), Eugene Gorbato, Ulf R. Hanebutte, Onur Mutlu. “Memory Power Management via Dynamic Voltage/Frequency Scaling.” In *8th IEEE/ACM International Conference on Autonomic Computing (ICAC)*, Karlsruhe, Germany, Jun. 2011.

- Chris Fallin, Chris Craik, Onur Mutlu. “CHIPPER: A Low-complexity Bufferless Deflection Router.” In *17th International IEEE Symposium on High Performance Computer Architecture (HPCA)*, San Antonio, TX, Feb. 2011.
- George Nychis, Chris Fallin, Thomas Moscibroda, Onur Mutlu. “Next-Generation On-Chip Networks: What Kind of Congestion Control Do We Need?” In *Ninth ACM Workshop on Hot Topics in Networks (HotNETS)*, Monterey, CA, Oct. 2010.

## Book Chapters

- Chris Fallin, Greg Nazario, Xiangyao Yu, Kevin Chang, Rachata Ausavarungnirun, Onur Mutlu. “Bufferless and Minimally-Buffered Deflection Routing” (book chapter). In *Routing Algorithms in Networks on-Chip*, pp. 241—275, Springer, 2014.

## Technical Reports

- Chris Fallin, Chris Wilkerson, Onur Mutlu. “The Heterogeneous Block Architecture.” SAFARI Technical Report No. 2014-001. March 13, 2014.
- Chris Fallin, Xiangyao Yu, Kevin Chang, Rachata Ausavarungnirun, Greg Nazario, Reetuparna Das, Onur Mutlu. “HiRD: A Low-Complexity, Energy-Efficient Hierarchical Ring Interconnect.” SAFARI Technical Report No. 2012-004: December 13, 2012.
- Chris Fallin, Greg Nazario, Xiangyao Yu, Kevin Chang, Rachata Ausavarungnirun, Onur Mutlu. “MinBD: A Minimally-Buffered Deflection Router Approaching Conventional Buffered-Router Performance.” SAFARI Technical Report No. 2011-008: September 13, 2011.
- Chris Fallin, Xiangyao Yu, Greg Nazario, Onur Mutlu. “A High-Performance Hierarchical Ring On-Chip Interconnect with Low-Cost Routers.” SAFARI Technical Report No. 2011-007: September 6, 2011.
- Kevin Chang, Rachata Ausavarungnirun, Chris Fallin, Onur Mutlu. “Adaptive Cluster Throttling: Improving High-Load Performance in Bufferless On-Chip Networks.” SAFARI Technical Report No. 2011-006: September 6, 2011.
- George Nychis, Chris Fallin, Thomas Moscibroda, Srinivasan Seshan, Onur Mutlu. “Congestion Control for Scalability in Bufferless On-Chip Networks.” SAFARI Technical Report No. 2011-003: July 20, 2011.
- Chris Fallin, Chris Craik, Onur Mutlu. “CHIPPER: A Low-complexity Bufferless Deflection Router.” SAFARI Technical Report No. 2010-001: December 29, 2010. (Extended version of our HPCA-17 conference paper.)

## Research Talks

- “weaving the wasms: AOT JS Compilation (or: Stuffing a Dynamic Language onto a Very Static Platform).” Wasm Research Day, Pittsburgh, PA, Jun. 2024.
- “weaving the wasms: AOT JS Compilation (or: Stuffing a Dynamic Language onto a Very Static Platform).” Carnegie Mellon University, Apr. 2024.
- “weaving the wasms: AOT JS Compilation (or: Stuffing a Dynamic Language onto a Very Static Platform).” PL Seminar, Northeastern University, Apr. 2024.
- “ægraphs: Acyclic E-graphs for Efficient Optimization in a Production Compiler.” Invited keynote at *EGRAPHS 2023* workshop at *PLDI*, Orlando, FL, Jun. 2023.
- “Finding and Exploiting Parallelism with Data-Structure-Aware Static and Dynamic Analysis.” *Thesis Defense*, CMU, Pittsburgh, PA, Feb. 2019.
- “Data-structure-aware program analysis for macro-scale optimizations.” *CMU PDL Fall Retreat*, Bedford Springs, PA, Oct. 2018.
- “Finding hidden concurrency: a data-structure-aware analysis for auto-parallelization.” *CMU PDL Fall Retreat*, Bedford Springs, PA, Oct. 2017.

- “Finding hidden concurrency: a data-structure-aware analysis for auto-parallelization.” *MIT-CMU Annual Parlay Meeting*, Cambridge, MA, Sep. 2017.
- “Macro-scale program optimizations by inferring semantic intent.” *CMU PDL Fall Retreat*, Bedford Springs, PA, Oct. 2016.
- “Heterogeneous Core Microarchitecture for Energy Efficiency.” *CMU CALCM (Computer Architecture Lab at Carnegie Mellon) Lecture*, Pittsburgh, PA, Apr. 2013.
- “Block-Based Heterogeneous Core Designs for Higher System Performance and Efficiency.” *Qualcomm Innovation Fellowship Finals*, San Diego, CA, Mar. 2013 (co-presented with Gennady Pekhimenko).
- “Enabling Fine-grained Heterogeneity with Atomic Blocks.” *Intel ARO Workshop*, Hillsboro, OR, Mar. 2013.
- “MinBD: Minimally-Buffered Deflection Routing for Energy-Efficient Interconnect.” *6th ACM/IEEE International Symposium on Networks-on-Chip (NOCS)*, Lyngby, Denmark, May 2012.
- “Memory Latency Tolerance: Skipahead & Efficient Runahead.” *Intel ARO Workshop*, Hillsboro, OR, Feb. 2012.
- “Memory Power Management via Dynamic Voltage/Frequency Scaling,” *8th IEEE/ACM International Conference on Autonomic Computing (ICAC)*, Karlsruhe, Germany, Jun. 2011.
- “CHIPPER: A Low-complexity Bufferless Deflection Router,” *17th International IEEE Symposium on High Performance Computer Architecture (HPCA)*, San Antonio, TX, Feb. 2011.

## Service

- External review committee for ASPLOS 2025.
- External review committee for ISCA 2024.

## Research Experience

- Post-doc for Prof. Todd Mowry and Prof. Phil Gibbons, CS, CMU, Mar 2019 – Jun 2019. Continuing thesis research on program analysis for parallelization and other transforms. Developed type-system approach to deriving program parallelizability.
- Ph.D. research assistant for Prof. Todd Mowry and Prof. Phil Gibbons, ECE, CMU, Jun 2015 – Feb 2019. Developing techniques for auto-parallelization and other high-level code transforms via static and dynamic code analysis.
- Ph.D. research assistant for Prof. Onur Mutlu, ECE, CMU, Aug 2009 – Jul 2013. Developed new energy-efficient core microarchitecture designs, energy-efficient network-on-chip designs, and memory system power scaling techniques.

## Teaching Experience

**Carnegie Mellon University**, spring 2010, spring 2012, Teaching Assistant, ECE Dept.

- TA for Introduction to Computer Architecture, 18-447, in spring 2012. Developed pipeline timing simulator in C and series of lab assignments, updated existing Verilog lab assignments, ran one lab session/recitation and held office hours, played major role in developing exams.
- TA for Parallel Comp. Arch., 18-742, in spring 2010. Mentored student research projects, delivered several lectures.

**University of Notre Dame**, spring 2008, fall 2008, spring 2009, Teaching Assistant, Computer Science & Engr. Dept.

- TA for Logic Design, CSE 20221, in spring 2008 and spring 2009. Graded homeworks and supervised one lab section.
- TA for Computer Architecture I, CSE 30321, in fall 2008. Supervised weekly lab, held office hours, wrote homeworks.

## Internships

**Intel Corporation**, Graduate Technical Intern (Hillsboro, OR), May – September 2012

- Worked in Intel Architecture Development Group on core architecture. Performed simulation studies to investigate mechanisms for memory latency tolerance.

**Intel Corporation**, Graduate Technical Intern (Hillsboro, OR), June – September 2010

- Conducted research in Power Management Architecture group, System Architecture Lab, Intel Labs.
- Evaluated mechanisms for processor and memory frequency and voltage scaling for server platforms. Resulted in ICAC 2011 publication on memory DVFS (dynamic voltage/frequency scaling).

**Cypress Semiconductor**, Undergraduate Co-op (Beaverton, OR), May – August 2007 and May – August 2008

- Worked on integrated development environment and EDA (electronic design automation) tools for programmable FPGA-like mixed analog/digital chips.
- Built generic design-rule check (DRC) framework to highlight errors in schematic design editor which became an user-visible feature in shipping software.

## Graduate Coursework

- CMU: Grad. Computer Architecture (ECE/CS), Advanced OS & Dist. Sys (CS), Algorithms in the Real World (CS), Optimizing Compilers (CS), Storage Systems (ECE), Analytical Performance Modeling (CS), VLSI CAD (ECE)
- ND: Graduate Algorithms (CSE)

## Research Fellowships

**SRC Graduate Research Fellowship**, Aug 2009 – Jul 2010. Awarded April 2009.

**NSF Graduate Research Fellowship**, Aug 2010 – Jul 2013. Awarded April 2009.

**Bertucci Fellowship**, 2013. Internal CMU College of Engineering fellowship. Awarded January 2013.

**Qualcomm Innovation Fellowship Honorable Mention**, 2013-2014 (with Gennady Pekhimenko). Awarded April 2013.

## Honors

- Distinguished Paper Award, ASPLOS 2023.
- One of five papers nominated for Best Paper Award, NOCS 2012.
- Steiner Award in Engineering, Notre Dame, April 2009  
(*awarded to one graduating senior in each engineering discipline*)
- Tau Beta Pi and Upsilon Pi Epsilon engineering honors societies
- Engineering Honors Program, Notre Dame
- Dean's List, all semesters at Notre Dame

## Professional Associations

- Member, Association for Computing Machinery (ACM) since Nov. 2006 (Full professional member since Mar. 2019)

## References

Available upon request.